# Lab Notebook <br> 27 Sept 2018 <br> EECT1112 

J eanie H., Caleb B.

## Index

O Lab 1 - Logic Levels Slide 3-6

O Lab 2 - Number Conversions Slide 7-15

○ Lab 3 - Logic Gates Slide 16-20

O Lab 4 - Lecture3bSlide3 Slide 21-26

O Lab 5 - Two Input Gates Slide 27-31

O Lab 6 - Theoroms Slide 32-35

O Lab 7 - Circuit Reduction Slide 36-40

- Lab 8-Circuit Reduction (Part 2) Slide 41-44
O Lab 9-1 to 3 clock using Jk Flip Flops and 555 Timers $\qquad$ Slide 45-48


## Lab 1 - Iogic Levels- 30 Aug 2018

O Purpose:
O Leam how to create logic levels for dig ital circ uits using switc hes and resistors.
O Equipment Used:

- Multisim

O 1- Digital multi-meter

- $4-10 \mathrm{k} \Omega$ resistors

O 1 - Position dip switch

## Lab 1 - Iogic levels

Step 1: Using Multisim program to create and simulate the following circuit in various positions.


## Lab 1 - Iogic levels

| Simulated |  |  |  |
| :---: | :---: | :---: | :---: |
| S1 | S2 | VA | VB |
| open | open | 4.999 V | 4.999 V |
| open | closed | 4.999 V | 50 nV |
| closed | open | 50 nV | 4.999 V |
| closed | closed | 50 nV | 50 nV |


| Test |  |  |  |
| :---: | :---: | :---: | :--- |
| S1 | S2 | VA | VB |
| open | open | 5 V | 5 V |
| open | closed | 5 V | .008 V |
| closed | open | .008 V | 5 V |
| closed | closed | .008 V | .008 V |

Table 1 (Simulation vs Test)
Step 2: Create the circ uit in the lab and take mea surements in va rious positions (No picture were taken during thislab).

Step 3: Display results in given tables.

| Simulated |  |  |  | Test |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| S3 | S4 | VC | VD | S3 | S4 | VC | VD |
| open | open | 499.945uV | 499.945 uV | open | open | . 008 V | . 008 V |
| open | closed | 499.945 uV | 5 V | open | closed | . 008 V | 5 V |
| closed | open | 5 V | 499.945 uV | closed | open | 5 V | . 008 V |
| closed | closed | 5 V | 5 V | closed | closed | 5 V | 5 V |

Table 2 (Simulation vs Test)

## Lab 1 - Logic levels

O One of the first things that was pointed out to us during this lab was we did not test the resistors foraccuracy before build ing our circ uit. Because of where the power source is placed is affecting how the power going through the resistors.

## Lab 2 - Number conversions - 9 Sept 2018

O Purpose:
O Leam how to convert numbers from one base to a nother.
O Equipment used:
O Excel
O Process:
O Using slides and excel sheets provided to fill in the valuesin the tablesincluding maxand mins of decimal values in different number bases.

## Lab 2 - Number Conversions

$5 \& 8$ bit Binary $\Rightarrow$ Decimal


## Summary

For each binary position that holds a ' 1 ' this value is held with a 2 to the power of the position. These powers sta rt at 0 on the furthest right position going up to the left. Therefore, the more bits you have the higher the powers will be. Once you have the all the 2's to the correct powerfor the ' 1 ' values of the bina ry you then add across to get the decimal value.

## Lab 2 - Number Conversions

Reverse Process


## Summary

Using the powers of 2 that will add up to the number that you start with in decimal to find which position of the ones and zeros in binary should be. So for every value of 2 that you do not use there will be a zero in that positions and a one for the positions that you use.

Ex: $32+8+4+1=45$

## Lab 2 - Number Conversions

Repeated Division


## Summary

Sta ring with a decimal number, you divide that by 2. If the result of this division is an whole number this leaves no remainder making the binary value for that position 0. If this result is not whole then there is a rema inder of one for the position. This process is repeated until you can no longer divide by 2.

## Lab 2 - Number Conversions

Hexadecimal Number System


## Summary

O Given the decimal number that needs to be converted to binary, take this number and divide it by 2. If the result of this division hasa number and a half keep the number and the half then tums to 1 in binary. That number that you have kept will then be divided. If there is no half for this division this keep that number and the binary will be a 0 .

## Lab 2 - Number Conversions

Hexto Decimal


## Summary

- Each place for the hex system is a position in decimalasa $16^{\text {ht }}$ to a powerforeach position. There is $1-9$ in the hex system then $10-15$ are replaced with letter A-F. So if you have a 2 in the first hex position then multiply this by 16 squared, then $A$ in the second position you must multiply 10 by 16 to the first and $F$ in the last position must multiply 15 by 16 to the zero.


## Lab 2 - Number Conversions

Decimal to hex


## Summary

- Take the given decimal number and divide it by 16 . this product should be an whole number so you must take out numbers until you receive a whole number as your answer. The numbers that you take out are then your remainder which will then be your number in hex for each position time that you divide by 16 if the remainder is $10-15$ if will then be replaced by A-F.


## Lab 2 - Number Conversions

| 378 | 17A |  |  |  | HEXBINARY |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 23.62523 |  | 7 | 10 | 0 | 0000 |  |  |
|  | 1.43751 |  |  |  | 1 | 0001 |  |  |
|  | 0.06250 | 1 |  |  | 2 | 0010 |  |  |
|  | Step 1 => | 1 | 7 | 10 | 3 | 0011 |  |  |
|  |  |  |  |  | 4 | 0100 |  |  |
|  | Step 2 => | 1 | 7 | A | 5 | 0101 |  |  |
|  |  |  |  |  | 6 | 0110 |  |  |
|  | Step 3 = | 001 | 0111 | 1010 | 7 | 0111 |  |  |
|  |  |  |  |  | 8 | 1000 | Max Decimal | 4095 |
|  | Step 4 = | 1 | 7 | A | 9 | $\begin{aligned} & 1001 \\ & 1010 \end{aligned}$ | value = |  |
|  |  |  |  |  | B | 1011 | Hexadecimal | FFF |
|  |  |  |  |  | C | 1100 | value $=$ |  |
|  |  |  |  |  | D | 1101 | Binary value = | 11111111 |
|  |  |  |  |  | F | 1111 |  | 1111 |

## Summary

- This method is using grouping of binary numbers to the comelating number in hex form. This would be similarto changing binary to decimal except for the numbers between $10-15$ will then be replaced with the letters between A-F


## Lab 2 - Number Conversions

O Observations
OThere are many ways to change the numbers from one counting system to another. Each system uses different types of polynomial functions to convert the numbers. It is interesting that there are different values that cannot be recognized in other systems of counting, once you type in something more than the max value it causes the equations to crash.

## Lab 3-Logic Gates-13 Sept 2018

O Purpose:
O Leam how to test AND and OR logic gates.

- Equipment used:

O 1 - Digital Multi-meter

- 2-10Kohm
- 1-4 position dip switch
- 1-74L508
- 1-74LS32


## Lab 3 - logic Gatas

Step 1: Using MultiSim to simulate the given circ uit in various positions with the AND gate and the OR gate.


## Lab 3 - logic Gatas

Step 2: Create real life wiring to simulate the wiring diagram made in MultiSim to compare results. We had to use Data sheets in order to wire these gates comectly.


## Lab 3-Logic Gates-Results

| AND Gate |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Smulated | Test |  |
| S1 | S2 | Output | Output |  |
| Open | Open | 5 | 4.176 |  |
| Open | Closed | 0 | 0.1436 |  |
| Closed | Open | 0 | 0.1436 |  |
| Closed | Closed | 0 | 0.1435 |  |


| OR Gate |  |  |  |
| :---: | :---: | :---: | :---: |
|  |  | Smulated | Test |
| S1 | S2 | Output | Output |
| Open | Open | 5 | 4.199 |
| Open | Closed | 5 | 4.199 |
| Closed | Open | 5 | 4.199 |
| Closed | Closed | 0 | 0.1351 |

## Lab 3-Iogic Gates

o Observation:
OThe first thing that we did was ensure that all the equipment was working properly by measuring resistor for proper tolerance. Power going into board is at 5.1 volts, showing power is dropping 1 volt through the circuit due to resistance and wiring. We notice the difference between the AND/OR gates: The AND gate only supplies power if both switches are closed and the OR gate supplies power as long at one switch is closed.

## Lab 4 - Lecture3bSide3 - 27 Sept 2018

O Purpose:
O Leam more a bout describing Logic Circ uits algebra ic a lly.
O Equipment:
○ 1 - Digital Multi-meter
O 3-10Kohm

- 4 - position dip switch
- 1-74LS08

○ 1-74LS32

## Lab 4 - <br> Lecture3bside3

Step 1: Creating the simulation given with inputs going first to the AND gate and than into the OR gate to measure output volta ge with a multimeter with various inputs.


## Lab 4 -

Lecture3bside3

Step 2: Creating the simulation given the inputs going first to the OR gate then going into the AND gate to read the output volta ge with the multimeter.


## Lab 4 -

lecture3bside3


Step 3: Create the simulation in the lab to compare the results. The data sheets were used as referencesto wire the AND/OR gates. We used the same set up foreach type of circuit then just switched the gates for the same wiring.

## Lab 4 - lecture3bSide3 - Results

| AND $\rightarrow$ OR |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | Simulated | Test |
|  |  |  | Output | Output |
| S1 | S2 | S3 |  |  |
| Open | Open | Open | 0 | 0.077 |
| Open | Open | Closed | 5 | 4.41 |
| Open | Closed | Open | 0 | 1.42 |
| Open | Closed | Closed | 5 | 4.41 |
| Closed | Open | Open | 0 | 1.51 |
| Closed | Open | Closed | 5 | 3.84 |
| Closed | Closed | Open | 5 | 4.40 |
| Closed | Closed | Closed | 5 | 4.40 |


| OR $\rightarrow$ AND |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | Smulated | Test |
|  |  |  | Output | Output |
| S1 | S2 | S3 |  |  |
| Open | Open | Open | 0 | 0.165 |
| Open | Open | Closed | 0 | 0.165 |
| Open | Closed | Open | 0 | 1.416 |
| Open | Closed | Closed | 5 | 4.38 |
| Closed | Open | Open | 0 | 1.42 |
| Closed | Open | Closed | 5 | 4.38 |
| Closed | Closed | Open | 0 | 1.40 |
| Closed | Closed | Closed | 5 | 4.38 |

## Lab 4 - Iecture33SSide3

O Observation:
ODuring the initial a ssembly of our of this circ uit we were getting bad reading. We spent time trouble shooting our whole circuit to find that that one of our gates were putting out bad values. This ended us with getting a new gate which fixes the error. Our values did seem to be jumping around quite a bit but everything was in spec of the highs and lows.

## Lab 5-Two Input Gates-4 Nov 2018

O Purpose:
O Leam how two input logic gates work using digital ICs, switc hes and resistors
O Equipment:
O 1 - Digital Multi-meter
O 2-10 kOhm resistors

- 1-4 position dip switch

○ 1- 74LS04, 74LS08, 74LS32, 74LS86

Step 1: Using MultiSim,
 create the given sc hematic, c reating two varying inputs for each gate being tested and take note of the outputs. In this case there are 4 possibilities.


Lab 5 - Iwo Input Gates
Step 2: Create the same circuit in the lab using the materials provided. Then compare the results to the simulation. This process inc luded using lab sheets to properly wiring different gates.


## Lab 5-Two inputgates-Results

| Simulated |  |  |  | Test |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{A}=$ |  |  | 0 | 0 | 1 | 1 | $\mathrm{~A}=$ | 0 | 0 | 1 |

O Our high reading was generally a round 4.2487 V and our low reading was a round 0.1055 V

## Lab 5 - Two input Gates

O Observations:
OThe gates acted just as we suspected they would. All the resistors and gates mea sured within there tolerance. We originally started with a large board finding this harder to follow and switch things a round. We then stuck with a small board only two gates at a time.

## Lab 6-Theorems-1 Nov 2018

O During this lab we used Excel, MultiSim and Lab time and space to prove the given theorems.
O All this information was provided in the midterm.
O The pictures from this lab will be provided in the following slides

## Iab 6 - Iheorems-Pictures



## Lab 6-Theorems- Pictures



## Lab 6 -Theorems



O Observations:
O All of the circuits built had the same expected results as the measured results.
O Having the expected results done before we went to the lab help ensure the we had built our circ uits properly.

## Lab 7 - Circuit Reduction - 8 Nov 2018

O Purpose:
O Leam how to reduce a circ uit design down to the smallest size using the 17 Theorems and Kamaugh maps. Part 2 will explore how to reduce the circ uit.
O Equipment used:
O 1- Digital Multi-meter
O 3-10kOhm Resistors

- 1-4 position dip switch

○ 1-74LS04, 74LS00, 74LS11, 74LS32

Step 1: Using the diagram provided, build circuit in MultiSim, simula ted expected results. With 3 inputs there are 8 possible outputs.


Step 2: Build the sa me circ uit in the lab comparing the results to the simulated products.


| Lab 7 - Circuit Reduction | Simulated |  |  |  | Test |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | B | C | Output |  | B | Output |  |  |  |  |  |
|  |  | 0 | 0 | 0 |  | 0 | 0.0679 |  |  |  |  |  |
| We gathered our results onto table comparing the numbers versus highs a nd lows. Using our new knowledge on reduction we created a Kamaugh Map as |  |  |  |  |  |  |  |  | BC |  |  |  |
|  | 0 | 0 | 1 | 0 |  | 01 | 0.068 |  | 00 | 01 | 11 | 10 |
|  |  | 1 | 0 | 0 |  | 10 | 0.0679 |  | 0.1 | 0.12 | 0.12 | 0.12 |
|  |  |  |  |  |  | 10 |  | 0 | 29 | 9 | 9 | 9 |
|  | 0 | 1 | 1 | 0 |  | 11 | 0.0678 | 1 | 4.4 | 4.47 | 0.12 | 4.47 |
|  |  | 0 | 0 | 0 |  | 0 | 4.335 |  |  |  |  |  |
|  |  | 0 | 1 | 0 |  | 01 | 14.3295 | $X=A B C+(A B)^{\prime}\left(A^{\prime} C^{\prime}\right)^{\prime}$ |  |  |  |  |
|  |  |  |  |  |  | 1 | 4.3295 | $X=A\left(B^{\prime}+C\right)$ |  |  |  |  |
|  |  | 1 | 0 | 0 |  | 10 | 0.0688 |  |  |  |  |  |
|  |  | 1 |  | 1 |  | 11 | 1.331 |  |  |  |  |  | formula.

## Lab 7 - Circuit Reduction

O Observations
O Finding ways to reduce circuit seems very useful because it was a lot more intricate for the full circ uit than for the reduction. Looking at the circuit like a math problem made the wiring and a nalyses much ea sier for me

## Lab 8 - Circuit Reduction (Part 2) - 15 Nov 2018

O Purpose:
O Leam how to reduce a circ uit design down to the smallest size using the 17 Theorems and Kamaugh maps. Part 2 will explore how to reduce the circuit. You will also need the results of Lab 7.
O Equipment used:
O 1 - Digital Multimeter
O 3-10Kohm
O 1-4 position dip switch
O 1-74LS04, 74LS08, 74LS32

Lab 8 - Circuit Reduction (Part2)

Using MultiSim we demonstrated the difference between a sum of products and a product of sum solution. I chose light to indic ate highs a nd lows for my switc hes.


Lab 8 - Circuit Reduction (Part 2)

Then we created the circ uits in the lab to compare the actual results.


## Lab 8 - Circuit Reduction (Part 2)

Results

| Simulation |  |  |  |  | Test |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Output |  |  |  |  | Output |  |
| A | B | C | SOP | POS | A | B | C | SOP | POS |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.1176 | 0.1186 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0.1176 | 0.1412 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0.1177 | 0.1417 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.1176 | 0.1419 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 4.221 | 4.354 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 4.22 | 4.352 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0.1146 | 0.1425 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4.219 | 4.349 |

## Observations

- We tried something in this lab with a light indic ator to give us an analog signal for on and off but for our sum of products in this lab the light affected our values. The light was dropping our output voltage dramatically.


## Lab 9-1 to 3 clock using Jk Fip Fops and 555 timers- 29 Nov 2018

O Pupose:
O Many times you can use multiple ha monic ally related clocks to test a combinational circ uits. The Pupose of this la b is to show students how to create a small multiple clock counter circ uit that usesJ K Flip Flops and a 555 Time
O Equipment Used:
O 1-555 Timer
○ 1-1Kohm

- 1-4 position dip switch

○ 2 - 74LS73 Dual J K flip flop with clear
○ 2 - Resistors (To Be Designed)
O 2 - Capacitors (To Be Designed)

Lab 9-1 to 3 clock using Jk Fip Fiops and 555 imers

Using the given information and diagrams to create the to use the interactive function in MultiSim to display the osc illosc ope.


Lab 9-1 to 3 clock using Jk Fip Fiops and 555 IImers

Then we created the sa me thing in the lab, lea ming to adjust the oscillosc ope to fit our needs. Also leaming to wire new types of gates.


## lab 9-1 to 3 clock using Jk Fip Fiops and 555 Timers

Results

|  | Designed | Measured |
| ---: | ---: | ---: |
| $\mathbf{R}_{\mathbf{A}}=$ | 470000 | 475000 |
| $\mathbf{R}_{\mathbf{B}}=$ | 470000 | 479000 |
| $\mathbf{C}=$ | 0.000001 | 0.000001 |
| $\mathbf{t}_{\mathbf{1}}=$ | 0.65142 | 0.661122 |
| $\mathbf{t}_{\mathbf{2}}=$ | 0.32571 | 0.331947 |
| $\mathbf{T}=$ | 0.97713 | 0.993069 |
| $\mathbf{f}=$ | 1.023405 | 1.0069794 |
| $\mathbf{f}=$ | 1.021277 | 1.0048849 |
| $\mathbf{D}=$ | $33.333 \%$ | $33.426 \%$ |

Observations
O Each clock is the next step in the binary count.

- The oscilloscope had to be adjusted from AC power to DC power.
O We had to change our switch to make the circuit functional
O Checking that everything is powered and grounded is essential.

